Claim Amendments

Claims 1, 2, and 5-7 have been amended. Claims 3, 4, 8, and 14-21 are canceled. Claims 9-13 are unchanged. The following listing of claims replaces all previous versions of the claims in the application.

Listing of Claims

1. (currently amended) A method for using a logic design system to implement a logic design in a programmable logic device, comprising:

using the logic design system to allow a logic designer to specify a desired logic design; and

generating configuration data for the programmable logic device using the logic design system that takes into account power consumption due to gate leakage effects, wherein the programmable logic device includes logic gates having stacks of transistors, the method further comprising using the logic design system to produce configuration data for the programmable logic device that configures the programmable logic device to route signals on the programmable logic device to positions within the stacks based on amounts that the signals are expected to be high or low.

2. (currently amended) The method defined in claim 1 ~~wherein there are signals on the programmable logic device, the method~~ further comprising using the logic design system to gather information on the signals from the logic designer.

3. canceled

4. canceled

5. (currently amended) The method defined in claim 1 ~~wherein there are signals on the programmable logic device, the method~~ further comprising analyzing the logic design with the logic design system to automatically generate information on the signals.

6. (currently amended) The method defined in claim 1 ~~wherein the programmable logic device includes logic gates containing stacks of transistors and wherein there are signals on the programmable logic device, the method~~ further comprising using the logic design system to produce configuration data that helps to reduce power consumption due to gate leakage effects in the programmable logic device by configuring the programmable logic device so that the signals that are handled by transistors that are higher in the stacks are more likely to be high than

signals that are handled by transistors that are lower in the stacks.

7. (currently amended) A method for using a logic design system to minimize power consumption in a programmable logic device, comprising:

using the logic design system to receive a desired logic design from a logic designer; and

producing configuration data for the programmable logic device with the logic design system that, when programmed into the programmable logic device, implements the desired logic design in the programmable logic device while routing signals on the programmable logic device to reduce power consumption due to gate leakage effects, wherein the programmable logic device includes logic gates having stacks of transistors with transistor gates and wherein producing the configuration data comprises producing configuration data that ensures that signals that are more likely to be high are routed to the transistor gates of the transistors higher in the stacks and that signals that are less likely to be high are routed to the transistor gates of the transistors lower in the stacks.

8. canceled.

9. (original) The method defined in claim 7 further comprising using the logic design system to receive a plurality of logic design constraints from the logic designer, wherein one of the constraints involves minimizing power consumption due to gate leakage effects and wherein producing the configuration data comprises producing configuration data that balances the plurality of constraints.

10. (original) The method defined in claim 7 wherein the programmable logic device includes at least one logic gate having a stack of transistors with transistor gates, wherein a first one of the transistors is higher in the stack than a second one of the transistors, and wherein first and second signals are received by the transistor gates, wherein the first signal is high more often than the second signal, and wherein producing the configuration data comprises producing configuration data that, when programmed into the programmable logic device, causes the first signal to be received by the first transistor gate and the second signal to be received by the second transistor gate to reduce power consumption due to gate leakage.

11. (original) The method defined in claim 10 further comprising using the logic design system to receive information

on the first and second signals from the logic designer, wherein the information on the first and second signals includes information that the first signal is high more often that the second signal.

12. (original) The method defined in claim 10 further comprising using the logic design system to automatically analyze the logic design to produce information that the first signal is high more often than the second signal.

13. (original) The method defined in claim 7 further comprising:

using the logic design system to gather signal type information from the logic designer; and

using the signal type information to determine how to route signals on the programmable logic device to minimize power consumption due to gate leakage.

14-21. canceled.